



FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Attorney Docket No.: 103-1	Application No.: 09/577,238
	Applicant: HO, Ying-Wai et al.	
	Filing Date: May 23, 2000	Group: 2124

Reference Designation	U.S. PATENT DOCUMENTS	Page 1
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Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
<u>CD</u> AA	5,631,859	5/1997	Markstein	364	748	10/27/1994
<u>CD</u> BB	5,652,875	7/1997	Taylor	395	500	5/24/1995
<u>CD</u> CC	5,671,170	9/1997	Markstein et al.	364	748	7/1/1994
<u>CD</u> DD	5,701,442	12/1994	Ronen	395	500	9/19/1995
<u>CD</u> EE	5,768,170	6/1998	Smith	364	748.1	7/25/1996
<u>CD</u> FF	5,995,122	11/1999	Hsieh et al.	345	523	4/30/1998
<u>CD</u> GG	5,996,066	11/1999	Yung	712	221	10/10/1996

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FOREIGN PATENT DOCUMENTS

Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)
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<u>CD</u> HH	Ito, Masayuki et al., "Efficient Initial Approximation for Multiplicative Division and Square Root by Multiplication with Operand Modification", IEEE Transactions on Computers, Vol. 46, No. 4, April 1997, pp. 495-498.

EXAMINER <u>[Signature]</u>	DATE CONSIDERED <u>8/13/03</u>
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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<p>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</p> <p><u>CD</u> Diefendorff, Keith et al., "AltiVec Extension to PowerPC Accelerates Media Processing," IEEE Micro, pp. 85-95, March-April 2000</p> <p><u>CD</u> AB Higaki et al., "A 2.5 GFLOPS 6.5 Million Polygons per Second 4-Way VLIW Geometry Processor with SIMD Instructions and a Software Bypass Mechanism," IEEE International Solid State Circuits Conference, 1999.</p> <p><u>CD</u> AC Kubosawa et al., "A 2.5-GFLOPS, 6.5 Million Polygons per Second, Four-Way VLIW Geometry Processor with SIMD Instructions and a Software Bypass Mechanism," IEEE Journal of Solid-State Circuits, Vol. 34, No. 11, pp. 1619-1626, November 1999</p> <p><u>CD</u> AD Kubosawa et al., "Four-Way VLIW Geometry Processor for 3D Graphics Applications," Fujitsu Sci. Tech. J., 36-1, pp. 39-47, June 2000 (manuscript received December 1, 1999)</p>			
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